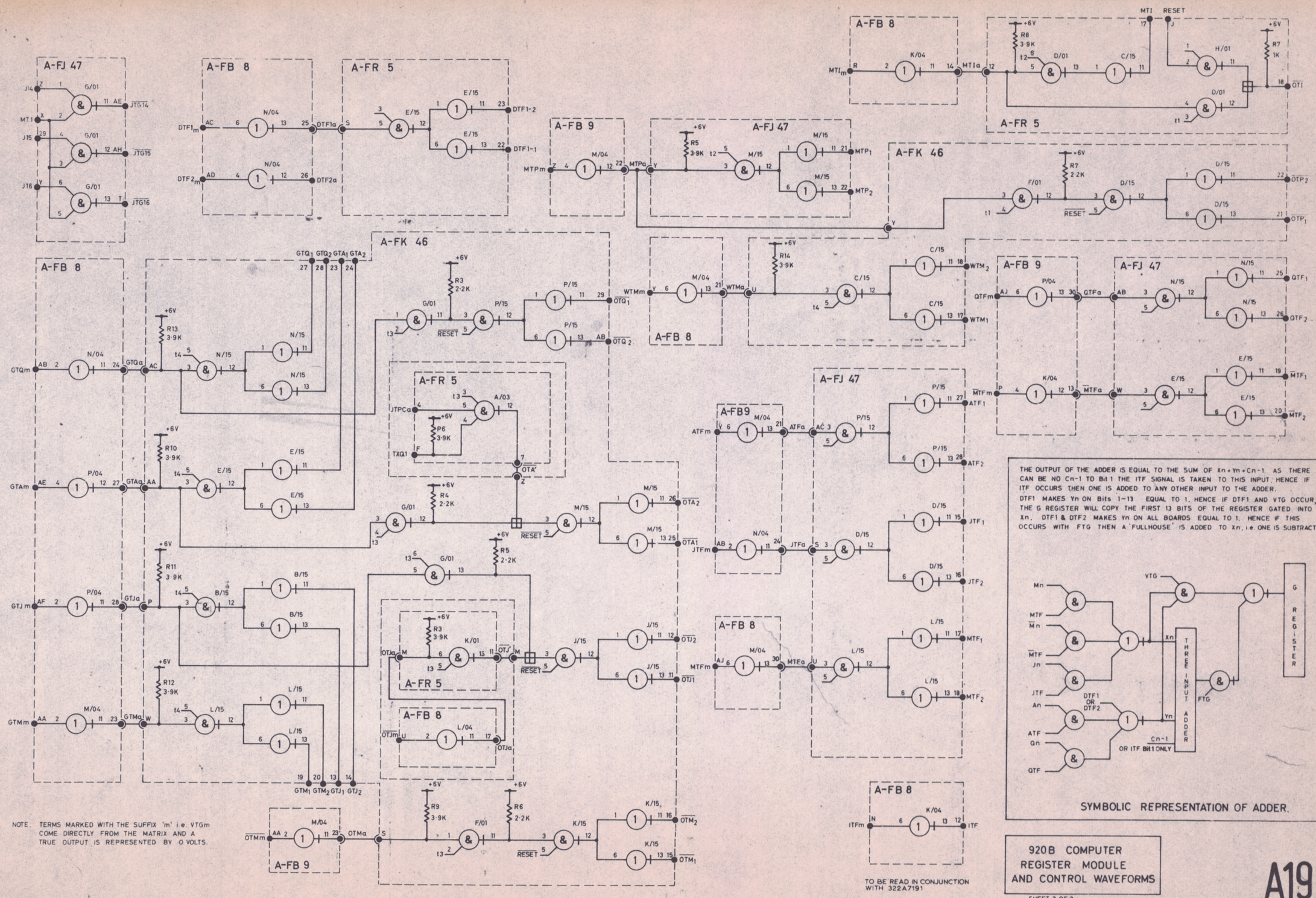
322 D7959 | THIRD ANGLE PROJECTION | DIMENSIONS IN INCHES UNLESS OTHERWISE STATED | DO NOT SCALE DRAWING



THE OUTPUT OF THE ADDER IS EQUAL TO THE SUM OF Xn + Yn + Cn-1. AS THERE CAN BE NO Cn-1 TO Bit 1 THE ITF SIGNAL IS TAKEN TO THIS INPUT. HENCE IF ITF OCCURS THEN ONE IS ADDED TO ANY OTHER INPUT TO THE ADDER.

DTF1 MAKES Yn ON Bits 1–13 EQUAL TO 1. HENCE IF DTF1 AND VTG OCCUR, THE G REGISTER WILL COPY THE FIRST 13 BITS OF THE REGISTER GATED INTO Xn. DTF1 & DTF2 MAKES Yn ON ALL BOARDS EQUAL TO 1. HENCE IF THIS OCCURS WITH FTG THEN A 'FULLHOUSE' IS ADDED TO Xn, i.e. ONE IS SUBTRACTED.

SYMBOLIC REPRESENTATION OF ADDER.

NOTE. TERMS MARKED WITH THE SUFFIX 'm' i.e. VTGm COME DIRECTLY FROM THE MATRIX AND A TRUE OUTPUT IS REPRESENTED BY 0 VOLTS.

TO BE READ IN CONJUNCTION WITH 322A7191

920B COMPUTER REGISTER MODULE AND CONTROL WAVEFORMS

SHEET 2 OF 2

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